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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/784,566	02/23/2004	Bo Jin	10002.003010 (CD03002)	8641

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EXAMINER	
HOLLINGTON, JERMELE M	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 08/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/784,566	JIN ET AL.	
	Examiner	Art Unit	
	Jermele M. Hollington	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-6,12 and 16-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 4-6, 12, and 16-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1 and 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cha et al (6849928) in view of Kurita (6753238).

Regarding claim 1, Cha et al disclose an anti-wafer structure [see Fig. 10] for testing a plurality of dice on a wafer under test, the structure comprising a silicon on insulator (SOI) layer (SOI layer 46); and a plurality of probe dice (pad 42) formed on the SOI layer (46), each probe

die in the plurality of probe dice having a pad layout corresponding lo a pad layout of a die on the wafer under test; a plurality of holes (holes 34 and 36) extending through the SOI layer (46) and the plurality of probe dice (42), the holes (34 and 36) corresponding to pads (42) on the probe dice. However, they do not disclose holes are filled with interconnect lines as claimed. Kurita disclose [see Figs. 6A-6D] a silicon on insulator layer (1), a plurality of probe dice (bump 4) on the SOI layer (1) and a plurality of holes (shown not number) extending through the plurality of probe dice (4) wherein the holes are filed with interconnect lines (interconnect lines 3). Further, Kurita teaches that the addition of interconnect lines inside holes is advantageous because cracks that are caused in a solder ball connection can significantly be reduced. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Cha et al by adding interconnect lines in holes extending through probe dice as taught by Kurita in order to significantly reduced cracks that are caused in a solder ball connection.

Regarding claim 4, Kurita disclose the interconnect lines (3) are coupled to pads (4) of the wafer under test (1).

Regarding claim 5, Cha et al disclose a number of the probe dice (42) equals a number of dice on the wafer under test.

Regarding claim 6, Cha et al disclose the SOI layer (46) comprises an oxide layer (oxide layer 14).

5. Claims are rejected under 35 U.S.C. 103(a) as being unpatentable over Cha et al (6849928) in view of S. Bengtsson et al (Interface charge control of directly bonded silicon structures).

Regarding claim 12, Cha et al disclose [see Fig. 10] a method of fabricating an anti-wafer, comprising providing a substrate (substrate 12), an SOI layer (SOI device 46 and 48) over the substrate (12), and a silicon layer (silicon layer 26) over the SOI layer (46), forming a seal layer (nitride layer 30) over the silicon layer (26); removing the substrate (12) using a polishing process (CMP polishing), forming an opening (openings 32, 34 and 36) through the SOI layer (46) and the silicon layer (26), and removing the seal layer (30), forming an interconnect line [via opening 32, 34 and 36] extending through the SOI layer (46) and the silicon layer (26). However, they do not disclose performing an HF dip process as claimed. Bengtsson et al disclose [see Journal of Applied Physics V66, pages 1233-1234 under "B. Sample preparation"] performing an HF dip process to clean a surface of the SOI layer after the polishing process. It is well known to clean the surface of the SOI layer using HF dip process as shown by Bengtsson et al in order to have good mechanical and electrical properties of the SOI layer.

Regarding claim 16, Cha et al disclose depositing [via chemical vapor deposition CVD] an oxide (oxide layer 28) on the SOI layer (46) after the HF dip process.

Regarding claim 17, Cha et al disclose the seal layer comprises: an oxide layer (oxide layer 28) over the silicon layer (silicon layer 26); and a nitride layer (nitride layer 30) over the oxide layer (28).

Regarding claim18, Cha et al disclose the silicon layer (26) includes pad openings (openings 34 and 36) and the seal layer (30) protects the pad openings (34 and 36) during subsequent processing steps.

Regarding claim 19, Cha et al disclose the SOI layer (46) comprises silicon dioxide (26).

Regarding claim 20, Cha et al disclose the substrate (12) comprises a silicon substrate.

Regarding claim 21, Cha et al disclose an anti-wafer structure [see Fig. 10] for testing a plurality of dice on a wafer under test, the structure comprising a silicon on insulator (SOI) layer (SOI layer 46); and a plurality of probe dice (pad 42) formed on the SOI layer (46), each probe die in the plurality of probe dice having a pad layout corresponding lo a pad layout of a die on the wafer under test. However, they do not disclose an adapter layer as disclose. Kurita disclose [see Figs. 6A-6D] a silicon on insulator layer (1), a plurality of probe dice (bump 4) on the SOI layer (1) and an adapter layer (resin layer 12) to adapt a pad layout of a probe dice (4). Further, Kurita teaches that the addition of adapter layer is advantageous because it improves the yield of the wafer without it being damage or breaking during the thinning process. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Cha et al by adding interconnect lines in holes extending through probe dice as taught by Kurita in order to significantly reduced cracks that are caused in a solder ball connection.

Regarding claim 22, Cha et al disclose a plurality of holes (holes 34 and 36) extending through the SOI layer (46) and the plurality of probe dice (42), the holes (34 and 36) corresponding to pads (42) on the probe dice.

Regarding claim 23, Kurita disclose [see Figs. 6A-6D] a silicon on insulator layer (1), a plurality of probe dice (bump 4) on the SOI layer (1) and a plurality of holes (shown not number) extending through the plurality of probe dice (4) wherein the holes are filed with interconnect lines (interconnect lines 3). Further, Kurita teaches that the addition of interconnect lines inside holes is advantageous because cracks that are caused in a solder ball connection can significantly be reduced. It would have been obvious to a person having ordinary skill in the art at the time the

invention was made to modify the apparatus of Cha et al by adding interconnect lines in holes extending through probe dice as taught by Kurita in order to significantly reduced cracks that are caused in a solder ball connection.

Regarding claim 24, Kurita disclose the interconnect lines (3) are coupled to pads (4) of the wafer under test (1).

Regarding claim 25, Cha et al disclose a number of the probe dice (42) equals a number of dice on the wafer under test.

Regarding claim 26, Cha et al disclose the SOI layer (46) comprises an oxide layer (oxide layer 14).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Spikes, Jr. et al (6074904), Beffa (6208947), Noble (6509213), Nulty et al (6847218), Ahn et al (6912778) disclose a method and apparatus for testing and manufacturing of a semiconductor device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (571) 272-1960. The examiner can normally be reached on M-F (9:00-4:30 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on (517) 272-2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jermele M. Hollington
Primary Examiner
Art Unit 2829

JMH
August 17, 2005